Reliability of Silver Wire Bonds

Matthew Parsons, Azzedin Jackson, Wenhao Chen, Alexander Campbell
Faculty Advisors: John Blendell, Carol Handwerker
Industrial Sponsors: Peng Su, Juniper Networks
Acknowledgements: Kathlene Reeve for assistance with SEM imaging

PURDUE MATERIALS ENGINEERING

Due to the price of gold and present difficulties with copper wire bonds in microelectronics, Juniper Networks is investigating silver as a replacement material for its wire bonded products. However, the reliability of silver wire bonds in microelectronics is not well quantified, raising concerns about the comparative reliability of the bonds over the lifetime of the product when compared to gold wire bonds. By performing accelerated testing and microstructure analysis on silver wire bonds, the reliability of silver wire bonds can be established and the suitability of silver as a gold replacement in semiconductor devices can be determined. The results show that silver wire bonds have an expected mean time to failure between 55.3 and 73.4 years.

This work is sponsored by Juniper Networks, based in Sunnyvale, California

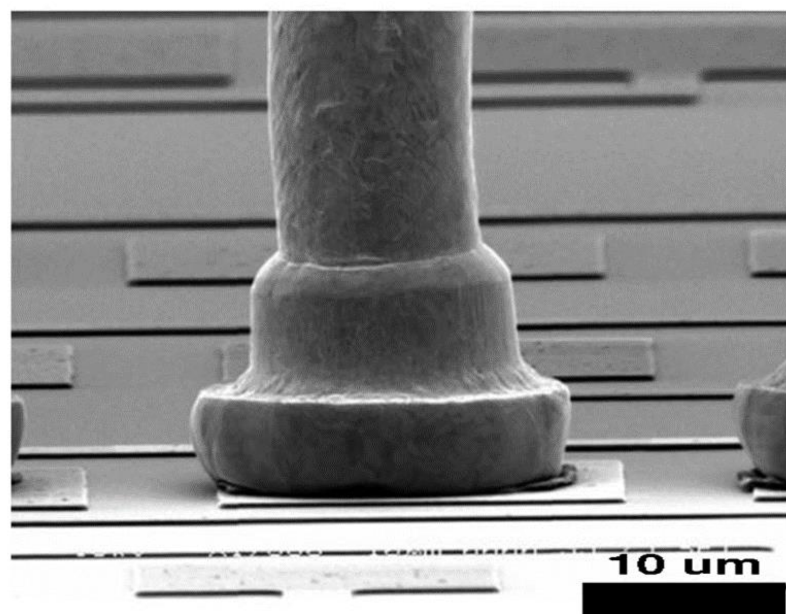
Project Background

Problem Statement

Wire bonds are an interconnect used to connect a microchip to external connectors that connect to a printed circuit board.

These wire bonds are often gold wire, but the price of gold has increased and fluctuates. Copper has been adopted as an alternative because it is significantly cheaper. However, copper was found to be too hard, which could lead to the component being damaged during wire bonding. Another alternative is silver, which is significantly cheaper than gold but much softer than copper. However, the reliability of silver wire bonds is poorly understood.

The goal of this project is to observe failure and quantify the life time of silver wire bonds using accelerated stress tests, and then compare the silver wire bonds to gold wire bonds.



A SEM Image of a wire bond[1].

A comparison of the material properties of gold, silver and copper[2].

Material Property	Ag	Au	Cu
Price ($/oz.)	1322.10	19.59	0.14
Thermal Conductivity (W/mK)	430	320	400
Electrical Resistivity ($10^{-8}\Omega m$)	1.63	2.2	1.72
Young's Modulus (GPa)	83	78	130
Vickers Hardness (MPa)	251	216	369

Failure Mechanisms

There are two main phenomena that contribute to wire bond failure – intermetallic compounds (IMCs) and corrosion.

Intermetallic compounds are formed when interdiffusion of metallic species occurs between the wire bond and bonding pad.

Corrosion occurs due to humidity and the presence of halogens in the molding compound surrounding the chip and its packaging.

During operation, IMCs grow and undergo corrosion reactions due to the presence of halogens. This leads to the formation of insulating alumina (Al_2O_3) and cracking that can disconnect the wire bond.

Reliability Testing

Accelerated stress tests are used to observe failure in shorter time spans and predicting lifetime. High Temperature Storage Testing (HTST) is used to monitor IMC growth at high temperature. Highly Accelerated Stress Testing (HAST) is used to monitor overall failure at high temperature, humidity, and applied bias on the wire bond.

Acceleration Factors are a multiplier that translates the time to failure under accelerated conditions to a lifetime prediction under normal operating conditions.

1. Goh, K S, and Z W Zhong. "Development of Capillaries for Wire Bonding of Low- K Ultra-Fine-Pitch Devices." 83.2006 (2014): 2009–2014. Web.
2. Chen, Q., Pagba, A., Reynoso, D., Thomas, S. & Toc, H. J. Cu wire and beyond – Ag wire an alternative to Cu ? in *12th Electronics Packaging Technology Conference* 591–596 (2010).

Experimental Procedure

7 different types of chips were purchased – 3 with silver wire bonds, 4 with gold wire bonds.

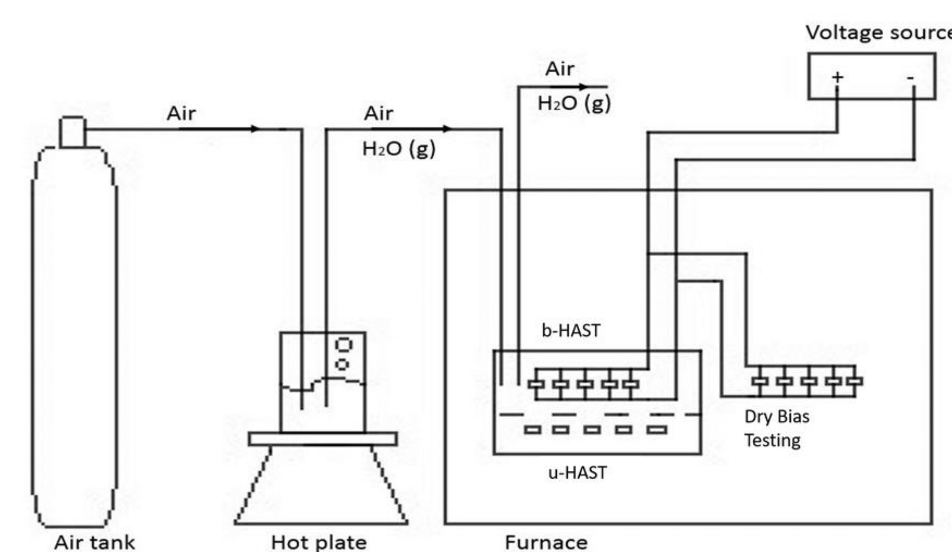
The resistance between selected leads established a baseline resistance.

Each chip type was tested in 4 different accelerated tests – HTST, biased (b-) Temperature-Humidity-Storage (THS), unbiased (u-)THS, and biased-HTST ("Dry Bias").

Chips were removed at different time intervals to track changes in resistance over time.

The resistance of the selected leads on each chip was measured to test for failure, which was defined as a 15% or greater increase in resistance[3].

The chips were mounted, polished, and analyzed using SEM to observe the microstructure.



Schematic of the experimental set up for b-THS, u-THS, and Dry Bias.

Test	Test Conditions	Chip Removal Times
HTST	• 150 ºC	• 500 Hours • 1000 Hours • 1500 Hours • 2000 Hours
Biased-HTST	• 130 ºC • 3.3 V bias	• 48 Hours • 96 Hours • 192 Hours • 288 Hours
u-THS	• 130 ºC • 85% Relative Humidity	• 96 Hours • 192 Hours • 288 Hours
b-THS	• 130 ºC • 85% Relative Humidity • 3.3 V bias	• 96 Hours • 192 Hours • 240 Hours • 288 Hours

3. Mayer, M., Xu, D. E. & Ratcliffe, K. The Electrical Reliability of Silver Wire Bonds under High Temperature Storage. (2016). doi:10.1109/ECTC.2016.347

Results And Discussion

The fraction of failed chip leads for HTST and Biased HTST for each testing duration. The input to ground leads are shown in **bold**.

Chip	Wire Bond Material	Leads Tested	Baseline (Ω)	Failure Resistance (Ω)	HTST 500 Hr	HTST 1000 Hr	HTST 1500 Hr	HTST 2000 Hr	Biased HTST 48 Hr	Biased HTST 96 Hr	Biased HTST 192 Hr	Biased HTST 288 Hr
Type 1	Silver	**1 and 3**	**0.37**	**0.44**	**0/5**	**0/5**	**0/5**	**0/5**	**3/3**	**0/3**	**1/3**	**0/3**
		1 and 4	5292	6350	4/5	5/5	5/5	5/5	1/3	3/3	2/3	2/3
		1 and 15	8200000	9840000	0/5	0/5	0/5	0/5	0/3	0/3	0/3	0/3
		1 and 37	4.88	5.86	0/5	0/5	0/5	0/5	0/3	0/3	1/3	0/3
Type 2	Gold	**3 and 6**	**15106000**	**18127200**	**0/5**	**3/5**	**5/5**	**5/5**	**0/3**	**3/3**	**3/3**	**3/3**
Type 3	Gold	**7 and 8**	**6330000**	**7596000**	**5/5**	**5/5**	**5/5**	**5/5**	**3/3**	**3/3**	**3/3**	**3/3**
Type 4	Gold	**2 and 5**	**587800**	**705360**	**0/5**	**0/5**	**0/5**	**0/5**	**0/2**	**0/3**	**0/3**	**1/3**
Type 5	Gold	1 and 3	2908000	3489600	0/5	0/5	0/5	0/5	0/3	0/3	0/3	0/3
		1 and 4	**3040000**	**3648000**	**0/5**	**0/5**	**0/5**	**0/5**	**0/3**	**0/3**	**0/3**	**0/3**
Type 6	Silver	1 and 2	58980	70776	0/5	0/5	0/5	0/5	0/3	0/3	0/3	0/2
		1 and 3	**22664**	**27197**	**0/5**	**0/5**	**0/5**	**0/5**	**0/3**	**0/3**	**0/3**	**0/2**
Type 7	SIlver	1 and 2	58040	69648	0/5	0/5	0/5	0/5	0/3	0/3	0/3	0/3
		1 and 3	**22856**	**27427**	**0/5**	**0/5**	**0/5**	**0/5**	**0/3**	**0/3**	**0/3**	**0/3**

The fraction of failed chip leads for u-THS and b-THS for each testing duration. The input to ground leads are shown in **bold**.

Chip	Wire Bond Material	Leads Tested	Baseline Resistance (Ω)	Failure Resistance (Ω)	u-THS 96 Hr	u-THS 196 Hr	u-THS 288 Hr	b-THS 96 Hr	b-THS 196 Hr	b-THS 240 Hr	b-THS 288 Hr
Type 1	Silver	**1 and 3**	**0.37**	**0.44**	**0/5**	**0/5**	**0/5**	**0/1**	**0/3**	----	**0/3**
		1 and 4	5292	6350	2/5	3/5	5/5	1/1	3/3	----	3/3
		1 and 15	8200000	9840000	0/5	0/5	0/5	0/1	0/1	----	0/3
		1 and 37	4.88	5.86	0/5	0/5	0/5	0/1	0/1	----	0/3
Type 2	Gold	**3 and 6**	**15106000**	**18127200**	**5/5**	**5/5**	**5/5**	-----	-----	-----	-----
Type 3	Gold	**7 and 8**	**6330000**	**7596000**	**5/5**	**5/5**	**5/5**	-----	-----	-----	-----
Type 4	Gold	**2 and 5**	**587800**	**705360**	**0/5**	**0/5**	**0/5**	**0/1**	**0/3**	----	**0/3**
Type 5	Gold	1 and 3	2908000	3489600	0/5	0/5	0/5	0/3	0/3	----	1/3
		1 and 4	**3040000**	**3648000**	**0/5**	**0/5**	**0/5**	**0/3**	**0/8**	**0/5**	**0/8**
Type 6	Silver	1 and 2	58980	70776	0/5	0/5	0/5	0/1	0/3	----	1/2
		1 and 3	**22664**	**27197**	**0/5**	**0/5**	**0/5**	**0/1**	**0/8**	**1/5**	**2/6**
Type 7	SIlver	1 and 2	58040	69648	0/5	0/5	0/5	0/1	0/3		0/3
		1 and 3	**22856**	**27427**	**0/5**	**0/5**	**0/5**	**0/1**	**1/8**	**0/4**	**2/8**

Results show that temperature, humidity, or bias (alone or in pairs) are not enough to cause failure in the time span of the test

All three in conjunction accelerate failure the most.

Under b-THS, silver chips fail at higher rates than gold chips – suggests lower reliability.

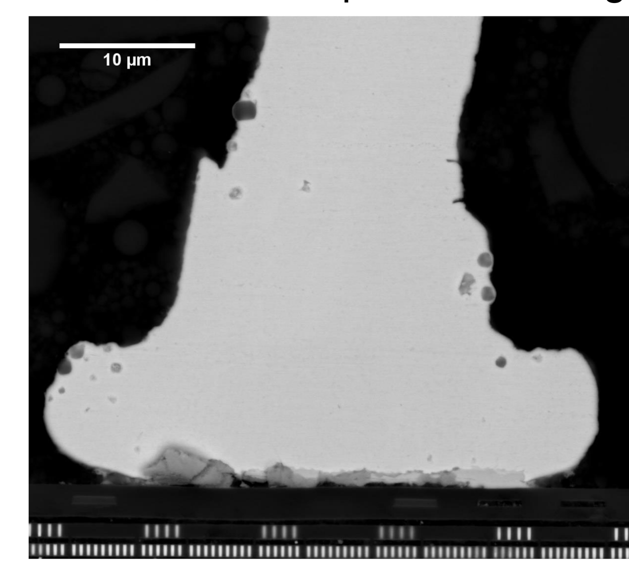
The Peck Equation, shown below, was used to calculate an Acceleration Factor (AF) of 337.92 for silver and gold based on our results. This translates to a lifetime of 7.4 to 10.8 years.

$$AF = \frac{V_{Test}}{V_{Use}}\left(\frac{RH_{Test}}{RH_{Use}}\right)^{n} e^{\left(\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{Test}}\right)\right)}$$

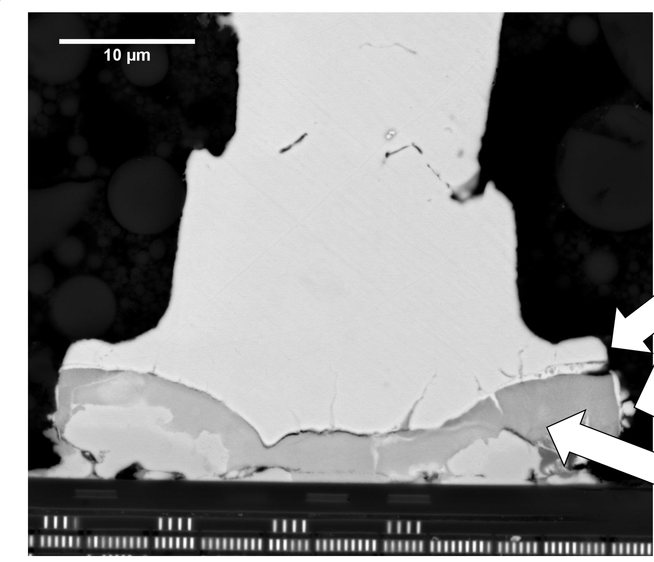
$$MTTF = \frac{AF * Total\ Device\ Test\ Hours\ * 2}{6.3}$$

The AF can be used to determine the mean time to failure (MTTF) for a population of chips based on the number of failures during testing.

Using this method and these results, a MTTF of 55.3 years was found for Type 6 chips and 73.4 years for Type 7 chips. No gold wire bond chips had a MTTF based on these results, as no chips failed during testing.

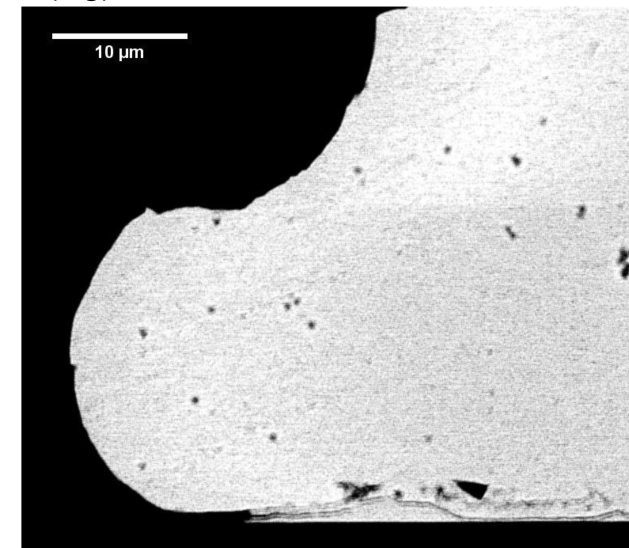


SEM micrograph of a failed Type 6 chip (Ag) that did not fail

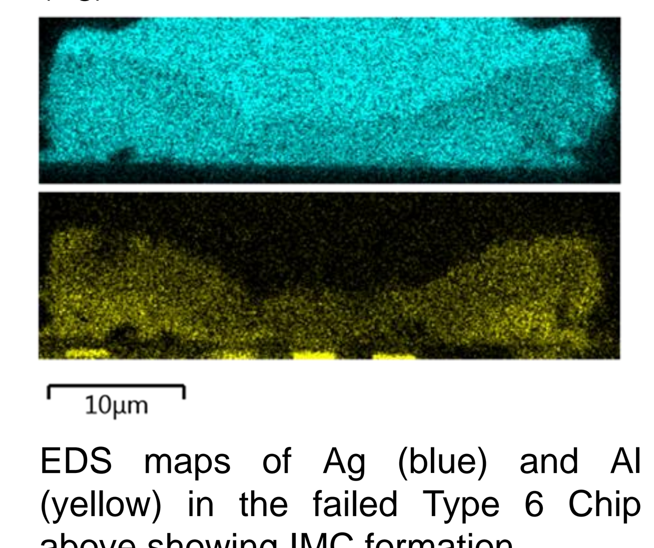


Crack
Corrosion
IMC

SEM micrograph of a Type 6 chip (Ag) that failed



SEM micrograph of a Type 5 chip (Au).



10µm

EDS maps of Ag (blue) and Al (yellow) in the failed Type 6 Chip above showing IMC formation.

Recommendations

Based upon the current results, silver wire bonds may satisfy requirements for chips that do not fail within 10 years. However, without a clearer comparison to the expected lifetime of gold wire bonds, either through more extreme accelerated testing or extending current testing, silver wire bonds do not represent a good replacement for gold wire bonds with concern to reliability. Further research should focus on characterization of the kinetics of the silver-aluminum system to determine the activation energy (E_a) of intermetallic formation, allowing for more accurate lifetime prediction.